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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Hao Fang et al.

Serial No.: 09/941,370

Filed: August 28, 2001

Group Art Unit: 2812

Before the Examiner: Richard A. Booth

Title: FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF

SUPPLEMENTAL APPEAL BRIEF

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is being submitted pursuant to 37 C.F.R. §1.193(b)(2)(ii). Appellants are furnishing herewith three (3) copies of this brief.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 13, 2004.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

I. INCORPORATION BY REFERENCE

The Appellants hereby incorporate herein by reference Sections I-V and VII-IX of Appellants' Appeal Brief mailed on July 22, 2003.

II. ISSUES

A. Is claim 1 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Cappelletti et al. (U.S. Patent No. 5,637,520) (hereinafter "Cappelletti") in view of Takebuchi (U.S. Patent No. 6,417,051) or Holler et al. (U.S. Patent No. 4,780,424) (hereinafter "Holler") or Wristers et al. (U.S. Patent No. 5,674,788) (hereinafter "Wristers")?

B. Are claims 2 and 10 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Cappelletti in view of Takebuchi, Holler or Wristers and further in view of Lee (U.S. Patent No. 5,175,120)?

III. GROUPING OF CLAIMS

Claims 2 and 10 form a first group.

Claim 1 should not be grouped and should be considered separately.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII of Appellants' Appeal Brief mailed on July 22, 2003 as well as in Section IV of Appellants' Supplemental Appeal Brief.

IV. ADDITIONAL ARGUMENTS

~~A. Claim 1 is not properly rejected under 35 U.S.C. §103(a) as being unpatenable over Cappelletti in view of Takebuchi, Holler or Wristers.~~

The Examiner has rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over Cappelletti in view of Takebuchi, Holler or Wristers. Paper No. 17, page 2.

1. The Examiner has not provided any objective evidence for combining Cappelletti with either Takebuchi, Holler or Wristers.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q. 2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying Cappelletti with either Takebuchi, Holler or Wristers to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area, as recited in claim 1, is to "allow[s] for a gate film of longer endurance." Paper No. 17, page 3. This motivation is insufficient to support a *prima facie* case of obviousness ~~since it is merely the Examiner's subjective opinion.~~

Cappelletti teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process. Column 5, lines 1-11.

Takebuchi, on the other hand, teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of a

tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET. Abstract.

Holler, on the other hand, teaches a process for fabricating contactless electrically programmable and electrically erasable memory cells of the flash EPROM type. Abstract. Holler further teaches that the contactless cells use elongated source and drain regions disposed beneath field oxide regions. Abstract. Holler further teaches that the drain regions are shallow compared to the source regions. Abstract. Holler further teaches that the source regions have more graded junctions. Abstract. Holler further teaches that floating gates are formed over a tunnel oxide between the source and drain regions with word lines being disposed perpendicular to the source and drain regions. Abstract.

Wristers, on the other hand, teaches a silicon oxynitride (oxynitride) dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. Abstract.

The Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with a reference (Takebuchi) that teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of a tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET, or with a reference (Holler) that teaches a process for fabricating contactless electrically programmable and electrically erasable memory cells, or with a reference (Wristers) that teaches an oxynitride (oxynitride) dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must

submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area. *Id.* Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to allow for a gate film of longer endurance. *Id.* Cappelletti makes no reference or suggestion to have a gate film of longer endurance and the Examiner has not provided any evidence as to why Cappelletti should be modified to allow for a gate film of longer endurance. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. M.P.E.P. §2143.

2. By combining Cappelletti with Takebuchi, the principle of operation of Cappelletti would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by combining Cappelletti with Takebuchi, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory. Accordingly, the Examiner has not presented a *prima facie* case of obviousness. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

Cappelletti teaches that according to Figure 10, a p-type substrate 30 has p-type wells 31; n-type wells 32; field insulating regions 34; channel stoppers 33; and a thin oxide layer 35'. Column 4, lines 20-23. Cappelletti further teaches that to obtain the required finish thickness of layer 35', a number of parameters are adjusted as compared with the known process described with reference to Figures 3-9. Column 4, lines 23-27. Cappelletti further teaches that using the same cell implant (EPM) mask 36, gate oxide layer 35' is etched and removed from cell area 40b', resulting in the intermediate structure shown in Figure 11. Column 4, lines 35-37. Cappelletti further teaches that at this time, EPM mask 36 is removed and the wafer is cleaned. Column 4, lines 37-38. Cappelletti further teaches that the wafer is oxidized to grow a thin oxide layer 61 directly on the surface of the substrate in cell area 40b', the oxidation parameters being selected to achieve the required characteristics, and particularly the thickness, of the thin tunnel oxide layer. Column 4, lines 38-43. Cappelletti further teaches that oxidation slightly increases the thickness of the gate oxide of the circuit transistors, as shown (exaggerated for clarity) by the dotted line in Figure 12 showing the original thickness of layer 35'. Column 4, lines 43-46. Cappelletti further teaches that the gate oxide layer on the circuit portion is indicated as 35" to take into account the increased thickness, though it is substantially equivalent to layer 35 in the known process. Column 4, lines 46-49. Cappelletti further teaches that the initial thickness of gate oxide layer 35' must be calculated to allow for the increase in tunnel oxidation and the slight reduction when the wafer is cleaned prior to forming the thin tunnel oxide. Column 4, lines 50-53.

Takebuchi, on the other hand, teaches a non-volatile memory element that includes a channel forming region formed by the p-type well region 31; a gate insulating film 60; a charge storing electrode 71; the tunnel insulating film 61; an n-type semiconductor region 51 for tunnel injection region (writing region) and removing region (erasing region) of charges as information; an intermediate gate insulating film 62; a control gate electrode 52 formed an n-type semiconductor

region; and a pair of n-type semiconductor regions 81 used as a source or drain region. Column 9, lines 41-50.

By combining Cappelletti with Takebuchi, Cappelletti would not be able to produce a flash-EEPROM memory using the DPCC process. Takebuchi does not teach increasing the thickness of the gate oxide of the circuit transistors. Instead, Takebuchi teaches a constant thickness for the gate insulating film. Consequently, the thickness of the gate oxide layer in Cappelletti would not be able to be produced with the required finish thickness. Hence, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory by combining Cappelletti with Takebuchi. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. M.P.E.P. §2143.

3. By combining Cappelletti with Holler, the principle of operation of Cappelletti would change.

As stated above, if the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by combining Cappelletti with Holler, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory. Accordingly, the Examiner has not presented a *prima facie* case of obviousness. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

As stated above, Cappelletti teaches that according to Figure 10, a p-type substrate 30 has p-type wells 31; n-type wells 32; field insulating regions 34; channel stoppers 33; and a thin oxide layer 35'. Column 4, lines 20-23. Cappelletti further teaches that to obtain the required finish thickness of layer 35', a number of parameters are adjusted as compared with the known process described with reference to Figures 3-9. Column 4, lines 23-27. Cappelletti further teaches that using the same cell implant (EPM) mask 36, gate oxide layer 35' is etched and removed from cell area 40b', resulting in the intermediate structure shown in Figure 11. Column 4, lines 35-37. Cappelletti further teaches that at this time, EPM mask 36 is removed and the wafer is cleaned. Column 4, lines 37-38. Cappelletti further teaches that the wafer is oxidized to grow a thin oxide layer 61 directly on the surface of the substrate in cell area 40b', the oxidation parameters being selected to achieve the required characteristics, and particularly the thickness, of the thin tunnel oxide layer. Column 4, lines 38-43. Cappelletti further teaches that oxidation slightly increases the thickness of the gate oxide of the circuit transistors, as shown (exaggerated for clarity) by the dotted line in Figure 12 showing the original thickness of layer 35'. Column 4, lines 43-46. Cappelletti further teaches that the gate oxide layer on the circuit portion is indicated as 35" to take into account the increased thickness, though it is substantially equivalent to layer 35 in the known process. Column 4, lines 46-49. Cappelletti further teaches that the initial thickness of gate oxide layer 35' must be calculated to allow for the increase in tunnel oxidation and the slight reduction when the wafer is cleaned prior to forming the thin tunnel oxide. Column 4, lines 50-53.

Holler, on the other hand, teaches nitride members 23 to prevent the formation of oxide in the channel regions 40. Column 4, lines 53-55. Holler further teaches that after the silicon nitride members 23 are removed, the substrate is subjected to a threshold voltage adjusting implant. Column 4, lines 66-68. Holler further teaches that Boron, as indicated by lines 36, is implanted to a level of approximately 1 x

$10^{13}/cm^2$. Column 4, line 68 – Column 5, line 1. Holler further teaches that the substrate is subjected to an etchant to remove the silicon dioxide layer from over the channel regions to permit growing of a high grade, gate oxide region over the channels. Column 5, lines 6-9.

By combining Cappelletti with Holler, Cappelletti would not be able to produce a flash-EEPROM memory using the DPCC process. Holler does not teach increasing the thickness of the gate oxide layer. Instead, Holler teaches forming a gate oxide region over the channels with a constant thickness. Consequently, the thickness of the gate oxide layer in Cappelletti would not be able to be produced with the required finish thickness. Hence, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory by combining Cappelletti with Holler. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. M.P.E.P. §2143.

4. By combining Cappelletti with Wristers, the principle of operation of Cappelletti would change.

As stated above, if the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by combining Cappelletti with Wristers, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory. Accordingly, the Examiner has not presented a *prima facie* case of

obviousness. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

As stated above, Cappelletti teaches that according to Figure 10, a p-type substrate 30 has p-type wells 31; n-type wells 32; field insulating regions 34; channel stoppers 33; and a thin oxide layer 35'. Column 4, lines 20-23. Cappelletti further teaches that to obtain the required finish thickness of layer 35', a number of parameters are adjusted as compared with the known process described with reference to Figures 3-9. Column 4, lines 23-27. Cappelletti further teaches that using the same cell implant (EPM) mask 36, gate oxide layer 35' is etched and removed from cell area 40b', resulting in the intermediate structure shown in Figure 11. Column 4, lines 35-37. Cappelletti further teaches that at this time, EPM mask 36 is removed and the wafer is cleaned. Column 4, lines 37-38. Cappelletti further teaches that the wafer is oxidized to grow a thin oxide layer 61 directly on the surface of the substrate in cell area 40b', the oxidation parameters being selected to achieve the required characteristics, and particularly the thickness, of the thin tunnel oxide layer. Column 4, lines 38-43. Cappelletti further teaches that oxidation slightly increases the thickness of the gate oxide of the circuit transistors, as shown (exaggerated for clarity) by the dotted line in Figure 12 showing the original thickness of layer 35'. Column 4, lines 43-46. Cappelletti further teaches that the gate oxide layer on the circuit portion is indicated as 35" to take into account the increased thickness, though it is substantially equivalent to layer 35 in the known process. Column 4, lines 46-49. Cappelletti further teaches that the initial thickness of gate oxide layer 35' must be calculated to allow for the increase in tunnel oxidation and the slight reduction when the wafer is cleaned prior to forming the thin tunnel oxide. Column 4, lines 50-53.

Wristers, on the other hand, teaches in Figure 14 how a fairly uniform concentration of nitrogen atoms in oxynitride dielectric layer 14 is capable of 1)

preventing boron atoms in polysilicon gate electrode 26 from penetrating into gate dielectric 28, and 2) preventing hot electrons from becoming trapped in gate dielectric 28. Column 8, lines 54-59. Wristers further teaches that a sufficient concentration of nitrogen atoms 48 in gate dielectric 28 near the interface between polysilicon gate electrode 26 and gate dielectric 28 (i.e., the polysilicon-dielectric interface) helps ensure boron atoms 50 in the overlying polysilicon gate electrode 26 are physically blocked by nitrogen atoms 48 in gate dielectric 28 and unable to penetrate into gate dielectric 28. Column 8, lines 59-65.

By combining Cappelletti with Wristers, Cappelletti would not be able to produce a flash-EEPROM memory using the DPCC process. Wristers does not teach increasing the thickness of the gate oxide layer. Instead, Wristers teaches a gate dielectric 28 with a concentration of nitrogen atoms 48 without increasing the thickness of the gate dielectric 28 via an oxidation step. Consequently, the thickness of the gate oxide layer in Cappelletti would not be able to be produced with the required finish thickness. Hence, the principle of operation in Cappelletti would change and subsequently render the operation of Cappelletti to perform its purpose unsatisfactory by combining Cappelletti with Wristers. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 1. M.P.E.P. §2143.

5. Cappelletti, Takebuchi, Holler and Wristers, taken singly or in combination, do not teach or suggest the following claim limitations.

Cappelletti, Takebuchi, Holler and Wristers, taken singly or in combination, do not teach or suggest "strengthening the interface by providing a nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area" as recited in claim 1. The Examiner cites column 12, lines 4-40 and Figures

4D-4F of Takebuchi as teaching the above-cited claim limitation. Paper No. 17, page 2. The Examiner further cites column 5, lines 12-15 of Holler as teaching the above-cited claim limitation. Paper No. 17, page 2. The Examiner further cites column 3, lines 40-65 of Wristers as teaching the above-cited claim limitation. Paper No. 17, page 2. Appellants respectfully traverse for at least the reasons stated below.

Appellants respectfully assert that Takebuchi instead teaches a substrate being nitrified in an NH_3 atmosphere. However, Takebuchi does not teach nitrifying the substrate after providing a portion of a dual gate oxide in a periphery area of a memory device and after simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area.

Appellants further assert that Holler instead teaches that the quality of a gate oxide layer may be enhanced by nitridation. However, there is no language in Holler that teaches nitridating the gate oxide layer after providing a portion of a dual gate oxide in a periphery area of a memory device and after simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area. Further, there is no teaching in Holler of nitridating the gate oxide layer in both a core and a periphery area of a memory device.

Appellants further assert that Wristers instead teaches there is an improvement in hot-carrier reliability of thermally-nitrided oxides attributed to the presence of nitrogen at the interface between a silicon substrate and a gate oxide. However, there is no language in Wristers that teaches introducing nitrogen at the interface after providing a portion of a dual gate oxide in a periphery area of a memory device and after simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area. Further, there is no teaching in Wristers of introducing nitrogen at the interface in both a core and a periphery area of a memory device.

Therefore, the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

B. Claims 2 and 10 are not properly rejected under 35 U.S.C. §103(a) as being unpatenable over Cappelletti in view of Takebuchi, Holler or Wristers and in further view of Lee.

The Examiner has rejected claims 2 and 10 under 35 U.S.C. §103(a) as being unpatentable over Cappelletti in view of Takebuchi, Holler or Wristers and in further view of Lee. Paper No. 17, page 3.

The Examiner has not provided any objective evidence for combining Cappelletti with either Takebuchi, Holler or Wristers and in further view of Lee.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

~~In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide~~ a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying Cappelletti with either Takebuchi, Holler or Wristers and in ~~further view of Lee to (1) deposit a layer of type-1 polysilicon in both a core area and~~ a periphery area of a memory device; (2) deposit a layer of oxide nitride oxide over

the layer of type-1 polysilicon; and (3) remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device, as recited in claims 2 and 10, is "because this is shown to be conventional fabrication for memory and peripheral circuits." This is not a motivation for modifying Cappelletti as described above. By not providing any motivation for modifying Cappelletti as described above, the Examiner has not provided a *prima facie* case of obviousness. M.P.E.P. §2142-2143.

As stated above, Cappelletti teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process. Column 5, lines 1-11.

As stated above, Takebuchi, on the other hand, teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of a tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET. Abstract.

As stated above, Holler, on the other hand, teaches a process for fabricating contactless electrically programmable and electrically erasable memory cells of the flash EPROM type. Abstract. Holler further teaches that the contactless cells use elongated source and drain regions disposed beneath field oxide regions. Abstract. Holler further teaches that the drain regions are shallow compared to the source regions. Abstract. Holler further teaches that the source regions have more graded junctions. Abstract. Holler further teaches that floating gates are formed over a tunnel oxide between the source and drain regions with word lines being disposed perpendicular to the source and drain regions. Abstract.

As stated above, Wristers, on the other hand, teaches a silicon oxynitride (oxynitride) dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. Abstract.

Lee, on the other hand, teaches simplifying the CMOS process by reducing the number of photomasks required as well as optimizing the n-channel implants of the array and periphery relative to one another. Column 7, lines 4-16.

The Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with a reference (Takebuchi) that teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of a tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET, or with a reference (Holler) that teaches a process for fabricating contactless electrically programmable and electrically erasable memory cells, or with a reference (Wristers) that teaches an oxynitride (oxynitride) dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate along with a reference (Lee) that teaches simplifying the CMOS process by reducing the number of photomasks required as well as optimizing the n-channel implants of the array and periphery relative to one another. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to deposit a layer of type-1 polysilicon in both a core area and a periphery area of a memory device. *Id.* Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon. *Id.* Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2 and 10. M.P.E.P. §2143.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Appellants

By: _____

Robert A. Voigt, Jr.
Reg. No. 47,159
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2832

AUSTIN_1\239626\1
184-P063D1